Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended): A method for reducing capacitance between interconnect lines, the method comprising:

providing a substrate having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon;

forming a metal layer over said substrate;

forming a pad oxide layer over said metal layer;

patterning and etching said pad oxide layer and metal layer to constitute said interconnect lines over said substrate;

forming an inter-metal dielectric layer over said substrate having said interconnect lines formed thereon~~, wherein~~ to form at least an air gap ~~is formed~~ in a spacing between the adjacent interconnect lines and below top surface of said pad oxide layer; and

planarizing said inter-metal dielectric layer without opening said air gap.

2. (Original): The method according to claim 1, wherein said metal layer is formed from materials selected from the group consisting of Al, Cu, Ta, W, Si, Au, Pb and Sn.

3. (Previously presented): The method according to claim 1, wherein the thickness of said pad oxide layer is between about 2000 angstrom and about 5000 angstrom.

4. (Original): The method according to claim 1, wherein said pad oxide layer comprises SiO_2, deposited by atmospheric pressure CVD method.

5. (Original): The method according to claim 1, wherein said pad oxide layer comprises SiO_2, deposited by plasma enhanced CVD method.

6. (Previously presented): The method according to claim 1, wherein said inter-metal dielectric layer comprises a SiO_2 layer, deposited by plasma enhanced CVD method, utilizing TEOS/O3 as a reaction gas.

7. (Previously presented): The method according to claim 1, wherein said inter-metal dielectric layer comprises a BPSG layer, deposited by atmospheric pressure CVD method, utilizing one of TEOS/O_3, TMPO and TEB as a reaction gas, at a temperature lower than 550□.

8. (Previously presented): The method according to claim 1, wherein said inter-metal dielectric layer comprises a BPSG layer, deposited by plasma enhanced CVD method, utilizing one of TEOS, O_3/O_2, TMP and TMB as a reaction gas, at a temperature between about 400□ and 500□.